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Filing Date	August 24, 2001
First Named Inventor	James M. Derderian
Art Unit	2826
Examiner Name	A. Williams
Attorney Docket Number	2269-4830US (01-0106.00/US)

ENCLOSURES ***(check all that apply)***

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☒ Appeal Brief; Claims Appendix
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below):*

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm	TraskBritt, P.C.		
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Date	January 18, 2007	Reg. No.	38,581

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

James M. Derderian

Serial No.: 09/939,253

Filed: August 24, 2001

For: SEMICONDUCTOR DEVICES AND SEMICONDUCTOR DEVICE ASSEMBLIES INCLUDING A NONCONFLUENT SPACER LAYER (AMENDED)

Confirmation No.: 2189

Examiner: A. Williams

Group Art Unit: 2826

Attorney Docket No.: 2269-4830US

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APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
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Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sir:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1). The required by 37 C.F.R. § 41.20(b)(2) has already been paid.

(I) REAL PARTY IN INTEREST

U.S. Application Serial No. 09/939,253 (hereinafter "the '253 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 012121, Frame No. 0076. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

(II) RELATED APPEALS AND INTERFERENCES

There are no related appeals, interferences, or other actions of which appellants or their attorneys are aware that may have a bearing on the outcome of the decision of the Board of Patent Appeals and Interferences (hereinafter "the Board") in the above-referenced appeal.

(III) STATUS OF CLAIMS

There are currently thirty-two (32) claims pending and under consideration in the '253 Application. All thirty-two claims stand finally rejected. The final rejections of the claims of the '253 Application are being appealed.

(IV) STATUS OF AMENDMENTS

The most recent claim amendments the '253 Application were introduced in an Amendment that was filed on January 26, 2006.

Despite detailed explanations as to the patentability of the claims under consideration, the rejections that had been presented prior to the Amendment of January 26, 2006, were maintained

in the final Office Action. Those rejections were again maintained in an Advisory Action dated June 28, 2006.

Accordingly, a Notice of Appeal was filed in the '253 Application on July 5, 2006, and was followed on September 27, 2006, by an Appeal Brief, along with a petition for a one month time extension and the appropriate fee. The Examiner mailed a Notice of Non-Compliant Appeal Brief on January 8, 2007. This Appeal Brief follows within one month of the date on which the Notice of Non-Compliant Appeal Brief was mailed.

(V) SUMMARY OF CLAIMED SUBJECT MATTER

While reference characters are used in the following summary to identify examples of claim elements that are shown in the drawings, it is noted that the reference characters are included merely to ensure full compliance with the requirements of 37 C.F.R. § 41.37(c)(1)(v), and that their inclusion merely points to examples in the as-filed disclosure that do not limit the scope of any claim that remains pending in the above-referenced application. Rather, the scope of each claim is limited only by the plain language thereof, and includes the full scope of available equivalents to each recited element.

Independent claim 1 of the '253 Application is directed to a semiconductor device 10, 10''' with a nonconfluent spacer layer 20. Paragraph **[0012]**; FIGs. 1-3, 9A, 9B. Such a spacer layer 20 may include one or more voids 24 that communicate with a lateral periphery of the spacer layer 20. *Id.* Claim 2, which depends from independent claim 1, is drawn to a semiconductor device with a spacer layer 20 that includes a plurality of laterally discrete spacers 22, 22'''. *Id.* As recited in claim 5, a thickness of the spacer layer 20 may exceed a

height that at least one intermediate conductive element (*e.g.*, a bond wire 18, etc.) protrudes above the active surface12, 12''' of the semiconductor device 10, 10''' to which the spacer 22, 22''' is secured. Paragraph **[0016]**; FIG. 9A. The spacer layer 20 may comprise a pattern, as recited in claim 8, which depends from independent claim 1, or randomly arranged features, as recited in claim 9, which also depends from independent claim 1. Paragraph **[0043]**.

Independent claim 19 is also directed to a semiconductor device 10, 10''' with a nonconfluent spacer layer 20. Paragraph **[0012]**; FIGs. 1-3, 9A, 9B. The nonconfluent spacer layer of claim 20, which depends from independent claim 19, includes one or more voids 24 that communicate with a lateral peripheral of the spacer layer 20. *Id.* Such a void 24 may be configured to facilitate introduction of adhesive material between adjacent, stacked semiconductor devices, as recited in dependent claim 21. Paragraph **[0012]**; FIGs. 9, 9C, 12. As recited in claim 22, the nonconfluent spacer layer 20 may comprise a plurality of laterally discrete spacers 22, 22'''. Paragraph **[0012]**; FIGs. 1-3, 9A, 9B. A thickness of the spacer layer 20 may exceed a height that at least one intermediate conductive element (*e.g.*, a bond wire 18, etc.) protrudes above the active surface of the semiconductor device 10, 10''' to which the spacer 22, 22''' is secured, as recited in claim 25. Paragraph **[0016]**; FIG. 9A. The spacer layer 20 may comprise a pattern, as recited in claim 33. Paragraph **[0043]**.

(VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) The 35 U.S.C. § 103(a) rejection of claims 1-10, 17, 19-26, 33, 37-39, and 42-44 for reciting subject matter that is assertedly unpatentable over the subject matter taught in U.S. Patent Publication 2001/0013643 of Nakanishi et al. (hereinafter "Nakanishi");

(B) The rejection of claims 11 and 12 under 35 U.S.C. § 103(a) for being drawn to subject matter that is allegedly not patentable over the teachings of Nakanishi, in view of teachings from U.S. Patent 6,049,370 to Smith, Jr., et al. (hereinafter "Smith");

(C) The rejection of claims 18 and 31 under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly unpatentable over the subject matter taught in Nakanishi, in view of teachings from U.S. Patent 5,220,200 to Blanton (hereinafter "Blanton"); and

(D) The 35 U.S.C. § 103(a) rejection of claims 11, 13, and 32 for reciting subject matter that is allegedly not patentable over teachings from Nakanishi, in view of the subject matter taught in U.S. Patent 6,316,786 to Mueller et al. (hereinafter "Mueller").

(VII) ARGUMENT

(A) CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 1-13, 17-26, 31-33, 37-39, and 42-44 stand rejected under 35 U.S.C. § 103(a).

(1) LEGAL AUTHORITY

The standard for establishing, maintaining, and upholding a rejection under 35 U.S.C. § 103(a) is set forth in M.P.E.P. § 706.02(j), which provides:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both

be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

(2) PRIMARY REFERENCE RELIED UPON

Nakanishi

The teachings of Nakanishi are limited to a polyimide spacer 24 (paragraph **[0078]**) that is "disposed along the periphery of the region where . . . semiconductor chips **1** and **2** are stacked" to provide for "a high level of accuracy in the balance of the intervals between the semiconductor chips **1** and **2**" (paragraph **[0080]**).

(3) ANALYSIS

(a) NAKANISHI

Claims 1-10, 17, 19-26, 33, 37-39, and 42-44 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter that is allegedly not patentable over the subject matter taught in Nakanishi.

The semiconductor device of independent claim 1 includes a dielectric spacer layer formed on and secured to at least a portion of a surface of a semiconductor die. The dielectric spacer layer includes "voids communicating with a lateral periphery thereof."

It is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1 because Nakanishi does not teach or suggest each and every element of independent claim 1. The teachings of Nakanishi are limited to an annular polyimide spacer 24 Nakanishi, paragraphs **[0078]** and **[0080]**. The annular configuration of the polyimide spacer 24 of Nakanishi is evident from the cross-sectional view provided by FIG. 9, in

which the polyimide spacer 24 is positioned adjacent to peripheral edges of the stacked assembly. As FIG. 9 is a cross section, it should be apparent to those of ordinary skill in the art that FIG. 9 does not illustrate the entire extent of the polyimide spacer 24. Thus, the drawings of Nakanishi do not illustrate an internal void that "communicate[s] with a lateral periphery" of the polyimide spacer 24. Further, the written disclosure of Nakanishi provides no teaching or suggestion that the internal void "communicate[s] with a lateral periphery" of the polyimide spacer 24.

As Nakanishi does not teach or suggest each and every element of independent claim 1, it is respectfully submitted that a *prima facie* case of obviousness has not been established against independent claim 1. As such, the subject matter to which independent claim 1 is directed is, under 35 U.S.C. § 103(a), allowable over the subject matter taught in Nakanishi.

Each of claims 2-10 and 17 is allowable, among other reasons, for depending directly or indirectly from claim 1, which is allowable.

Claim 2 is further allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof may include a plurality of laterally discrete spacers.

Claim 5 is also allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof may have a thickness that exceeds a height that at least one intermediate conductive element (*e.g.*, bond wires 8a, 8b of FIG. 9) protrudes above the active surface of a semiconductor device 2, 3 to which the polyimide spacer is secured.

Claim 8 is additionally allowable because Nakanishi teach or suggest that the polyimide spacer 24 thereof comprises a pattern.

Claim 9 is further allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof comprises randomly arranged features.

Claim 17 is also allowable because Nakanishi does not teach or suggest that adhesive material may be present on an exposed surface of the polyimide spacer 24.

It is also respectfully submitted that the teachings of Nakanishi do not support a *prima facie* case of obviousness against independent claim 19. Independent claim 19 recites a semiconductor device assembly that includes, among other things, a nonconfluent spacer layer that spaces an active surface of a first semiconductor device apart from a back side of a second semiconductor device.

The teachings of Nakanishi are limited to assemblies with spacer layers that separate active surfaces of semiconductor devices from one another. *See, e.g.,* Fig. 9; paragraphs **[0077]** and **[0047]**. As Nakanishi does not teach or suggest an assembly in which a spacer layer spaces an active surface of a first semiconductor device apart from a back side of a second semiconductor device, Nakanishi cannot be relied upon to establish a *prima facie* case of obviousness against independent claim 19.

Therefore, under 35 U.S.C. § 103(a), the subject matter recited in independent claim 19 is allowable over the subject matter taught in Nakanishi.

Claims 20-26, 33, 37-39, and 42-44 are each allowable, among other reasons, for depending directly or indirectly from claim 19, which is allowable.

Claim 20 is also allowable since Nakanishi neither teaches nor suggests that the polyimide spacer 24 thereof includes at least one void that communicates with a lateral periphery of the polyimide spacer 24.

Claim 21, which depends from claim 20, is additionally allowable because Nakanishi does not teach or suggest that the polyimide spacer 24 includes a void that facilitates introduction of adhesive material between first and second semiconductor devices.

Claim 22 is further allowable since Nakanishi includes no teaching or suggestion that the polyimide spacer 24 thereof includes a plurality of laterally discrete spacers.

Claim 24 is additionally allowable because Nakanishi does not teach or suggest an assembly in which an intermediate conductive element is located at least partially between first and second semiconductor devices that are spaced apart from one another by the polyimide spacer 24 disclosed therein.

Claim 25 depends from claim 24 and is also allowable since Nakanishi lacks any teaching or suggestion that the polyimide spacer 24 thereof may space first and second semiconductor devices apart from one another a distance that exceeds a height that at least one intermediate conductive element (*e.g.*, bond wires 8a, 8b of FIG. 9) protrudes above the active surface of one of the semiconductor devices 2, 3.

Claim 33 is additionally allowable because Nakanishi teach or suggest that the polyimide spacer 24 thereof comprises a pattern.

(b) NAKANISHI IN VIEW OF SMITH

Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) for reciting subject matter which is assertedly unpatentable over that taught in Nakanishi, in view of teachings from Smith.

Claims 11 and 12 are allowable, among other reasons, for depending from claim 1, which is allowable.

(c) NAKANISHI IN VIEW OF BLANTON

Claims 18 and 31 have been rejected under 35 U.S.C. § 103(a) for reciting subject matter which is allegedly unpatentable over the subject matter taught in Nakanishi, in view of teachings from Blanton.

Claim 18 is allowable, among other reasons, for depending from claim 1, which is allowable.

Claim 31 is allowable, among other reasons, for depending from claim 19, which is allowable.

(d) NAKANISHI IN VIEW OF MUELLER

Claims 11, 13, and 32 stand rejected under 35 U.S.C. § 103(a) for being directed to subject matter that is purportedly not patentable over the subject matter taught in Nakanishi, in view of the teachings of Mueller.

Claims 11 and 13 are both allowable, among other reasons, for depending directly from claim 1, which is allowable.

Claim 32 is allowable, among other reasons, for depending directly from claim 19, which is allowable.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-13, 17-26, 31-33, 37-39, and 42-44 be withdrawn.

(B) ELECTION OF SPECIES REQUIREMENT

Independent claim 1 remains generic to all of the species of invention that were identified in the Election of Species Requirement in the '253 Application. In view of the allowability of these claims, claims 14-16, 27-30, 34-36, 41, and 45-67, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

(VIII) CLAIMS APPENDIX

Each claim that has been considered in the '253 Application is set forth in CLAIMS APPENDIX to this Appeal Brief.

(IX) EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

(X) RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

(XI) CONCLUSION

It is respectfully submitted that:

(A) Claims 1-10, 17, 19-26, 33, 37-39, and 42-44 are allowable under 35 U.S.C. § 103(a) for reciting subject matter that is patentable over the subject matter taught in Nakanishi;

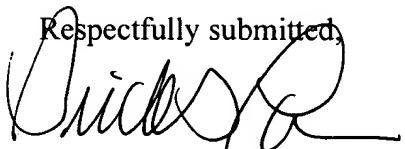
(B) Claims 11 and 12 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter that is patentable over the teachings of Nakanishi and Smith;

(C) Claims 18 and 31 are allowable under 35 U.S.C. § 103(a) for being directed to subject matter that is patentable over the subject matter taught in Nakanishi and Blanton; and

(D) Claims 11, 13, and 32 are allowable under 35 U.S.C. § 103(a) for reciting subject matter that is patentable over teachings from Nakanishi and Mueller.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 1-13, 17-26, 31-33, 37-39, and 42-44 be reversed, and that each of these claims be allowed. Further, as independent claim 1 remains generic to all of the species of invention that were identified in the Election of Species Requirement in the '253 Application, it is respectfully requested that claims 14-16, 27-30, 34-36, 41, and 45-67 be considered and allowed.

Respectfully submitted,



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CLAIMS APPENDIX

1. A semiconductor device for use in a stacked multi-chip assembly, comprising:

a semiconductor die; and

a dielectric spacer layer formed on and secured to at least a portion of a surface of the semiconductor die and protruding from the surface to space the semiconductor die substantially a predetermined distance from an adjacent semiconductor die to accommodate a height of at least one intermediate conductive element between the semiconductor die and the adjacent semiconductor die, the dielectric spacer layer protruding from the surface substantially the predetermined distance before at least one intermediate conductive element is secured to a bond pad of the semiconductor die, the spacer layer including voids communicating with a lateral periphery thereof.

2. The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a plurality of laterally discrete spacers.

3. The semiconductor device of claim 1, further comprising:

at least one discrete conductive element protruding above a surface of the semiconductor die.

4. The semiconductor device of claim 3, wherein the at least one discrete conductive element comprises one of a bond wire, a thermocompression bonded lead, and a tape-automated bond element.

5. The semiconductor device of claim 1, wherein the predetermined distance exceeds a distance a discrete conductive element protrudes above a surface of at least one of the semiconductor die and the adjacent semiconductor die.

6. The semiconductor device of claim 1, wherein the predetermined distance is about the same as or less than a distance a discrete conductive element protrudes above a surface of at least one of the semiconductor die and the adjacent semiconductor die.

7. The semiconductor device of claim 1, wherein the dielectric spacer layer covers only a portion of the surface.

8. The semiconductor device of claim 7, wherein the dielectric spacer layer comprises a pattern.

9. The semiconductor device of claim 7, wherein the dielectric spacer layer comprises randomly arranged features.

10. The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a material that will adhere to a surface of the adjacent semiconductor die.

11. The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a polymer.

12. The semiconductor device of claim 11, wherein the polymer comprises a photoimageable polymer.

13. The semiconductor device of claim 1, wherein the dielectric spacer layer comprises at least one of a glass, a silicon dioxide, a silicon nitride, and a silicon oxynitride.

17. The semiconductor device of claim 1, further comprising:

adhesive material on an exposed surface of the dielectric spacer layer.

18. The semiconductor device of claim 1, wherein the dielectric spacer layer comprises a plurality of at least partially superimposed, contiguous, adhered sublayers.

19. A semiconductor device assembly, comprising:

a first semiconductor device including an active surface carrying bond pads that are configured to have intermediate conductive elements secured thereto;

a nonconfluent spacer layer comprising dielectric material secured to the active surface of the first semiconductor device and, prior to securing an intermediate conductive element to any of the bond pads, protruding from the active surface substantially a same distance the active surface of the first semiconductor device is to be spaced apart from a back side of a second semiconductor device; and

the second semiconductor device, including a back side secured to the nonconfluent spacer layer.

20. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises at least one void therein that communicates with a lateral periphery of the nonconfluent spacer layer.

21. The semiconductor device assembly of claim 20, wherein the at least one void facilitates lateral introduction of adhesive material between the first and second semiconductor devices.

22. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a plurality of laterally discrete spacers.

23. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer has a substantially uniform thickness.

24. The semiconductor device assembly of claim 19, further comprising:

at least one intermediate conductive element protruding above the active surface of the first semiconductor device and located at least partially between the first and second semiconductor devices.

25. The semiconductor device assembly of claim 24, wherein the nonconfluent spacer layer has a thickness that spaces the first and second semiconductor devices apart from one

another a distance that exceeds a height the at least one intermediate conductive element protrudes above the active surface of the first semiconductor device.

26. The semiconductor device assembly of claim 24, wherein the nonconfluent spacer layer has a thickness that spaces the first and second semiconductor devices apart from one another a distance that is about the same as or less than a height the at least one discrete conductive element protrudes above the active surface of the first semiconductor device.

31. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a plurality of at least partially superimposed, contiguous, mutually adhered sublayers.

32. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises at least one of a glass, a silicon oxide, a silicon nitride, and a silicon oxynitride.

33. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a pattern.

37. The semiconductor device assembly of claim 19, further comprising:
a substrate upon which the first semiconductor device is positioned.

38. The semiconductor device assembly of claim 37, wherein at least one bond pad of at least one of the first semiconductor device and the second semiconductor device is in communication with a corresponding contact area of the substrate.

39. The semiconductor device assembly of claim 37, wherein the substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

42. The semiconductor device assembly of claim 19, wherein the nonconfluent spacer layer comprises a plurality layers, additive thicknesses of the plurality of layers defining substantially the same distance.

43. The semiconductor device assembly of claim 42, wherein a first layer of the plurality of layers is secured to the active surface of the first semiconductor device and a second layer of the plurality of layers is configured to be secured to the back side of the second semiconductor device.

44. The semiconductor device assembly of claim 42, wherein at least some solid regions of each of the plurality of layers are at least partially superimposed relative to one another.